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Design of High Throughput MIMO Detectors with Hardware Efficient Architecture

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Abstract— MIMO-OFDM is the foundation for most advanced wireless local area network (Wireless LAN) and mobile broadband network standards. The efficient architecture of 4*4 64-QAM MIMO detectors are mainly used for the wireless communication. The existing architecture embedded large number of buffer memories ,increases the chip area and power consumption. In order to reduce the area and power consumption novel error-resilient k-best MIMO detector architecture is used. This paper concentrates to modify the IPM processor and the PCM blocks in MIMO detector architecture. This optimization technique to reduce the power consumption and increase the speed also. The two-way sorting approach mainly used to reduce the power consumption level and also reduce the circuit complexity. This methodology to reduce the internal component level and to design the internal component in tree formation process and modified the child process. And find the minimum distance in the gate component architecture. MIMO detector architecture Synthesis and implementation is done by using Xilinx 14.2i Spartan 3E kit.

Keywords*:* VLSI, MIMODETECTOR, IPM, PCM